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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/710,606	11/10/2000	Jong-Myoung Lee	AB-1060 US	5064

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/710,606	Lee
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 29, 2002*.

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-5* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 3
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Russell (US Pat. 5545920) in view of Tsubosaki et al (US Pat. 6137159) and Takeuchi (US Pat. 5977614).

Regarding claim 1, Russell discloses Lead-on-chip (LOC) semiconductor package comprising:

- a semiconductor chip (12 in Fig. 5) on which a plurality of bonding pads (121/51 in Fig. 5) are arranged in rows
- leads (102/52 in Fig. 5) corresponding to the bonding pads being located on the opposite sides of the chip with the bonding pads therebetween (Fig. 5)
- wires (14 in Fig. 5) electrically connecting the bonding pads and the leads

- a molding resin (15 in Fig. 1-5) encapsulating the chip, leads and wires where the leads include a plurality of general/conducting leads (52 outside the chip in Fig. 5) and support/conducting leads (101/102 in Fig. 5)

- the support leads being electrically connected to the bonding pads via the wires (4 in Fig. 15) and bent to extend toward the chip and having ends of the leads being conventionally attached/physically affixed to the chip with an adhesive member (Col. 3, line 50)

- the general/conducting leads being disposed in a row between the support/conducting leads (leads 52 between leads 102 at the corner of the chip in Fig. 5) and being electrically connected to the bonding pads via the wires and separated from the chip without being into physical contact with the chip

(Fig. 5; Fig. 1-5; Col. 3, line 30 Col. 4, line 50).

Russell fails to specify/label the support/conducting leads as stable leads and those being at most four stable leads.

However, Russell further discloses using a conventional two-sided adhesive tape/member (11 in Fig. 1A/C; Col. 3, line 50) on a portion of the surface of the chip to fix the chip to the corresponding portions of the end of each of the support/conducting inner leads. It would have been obvious to one of ordinary skill that such

support/conducting leads physically contacting the chip provide the function of stabilizing and supporting the package.

Tsubosaki et al teach using a variety of configurations of a LOC device having support/stable/bus bar leads and general leads where the LOC device is supported by two support/stable leads (3C in Fig. 15 and 17; Col. 9, line 60- Col. 10, line 25).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at most four stable leads so that the mechanical stress can be reduced and the resin sealing can be improved using Tsubosaki et al's lead structure in Russell's package.

Regarding claim 2, Russell further discloses the general/conducting leads and support/conducting leads comprising inner and outer lead/portions where the inner leads are encapsulated in the molding resin and the outer leads extend from the molding resin (Fig. 5 and 1A-C; Col. 3, line 52).

Regarding claim 3, the claim elements have been addressed in the rejections as explained above for claims 1 and 2.

Regarding claim 4, Russell fails to specify a surface area of the end of the stable inner lead contacting the adhesive member being substantially wider/greater than a portion of the stable inner lead not in contact with the adhesive.

Takeuchi discloses the power/stable inner leads having a zig-zag shape configuration such that the dimension/area of the end of the power/stable inner lead (35a in Fig. 6) contacting the adhesive member is substantially wider/greater than a portion of the stable inner lead not in contact with the adhesive (Col. 6, line 50; Col. 7, line 32).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the stable inner leads where the surface area of the end of the stable inner lead contacting the adhesive member is substantially greater than a portion of the stable inner leads which is not in contact with the adhesive so that the lead strength and adhesion can be improved using Takeuchi and Tsubosaki et al's lead structure in Russell's package.

Regarding claim 5, Russell fails to specify the ends of the general inner leads being up-set toward the top of the chip.

It is a matter of design choice in chip packaging and interconnection technology art to select the configuration of the general leads extending from the package such as

up-set, down-set, co-planar, etc. to achieve the desired layout for an external connection.

Tsubosaki et al teach using a conventional up-set configuration for the general leads (Fig. 2; Col. 4) in a LOC package.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate general inner leads having an up-set configuration toward the top of the chip to facilitate subsequent mounting/connection using Tsubosaki et al and Takeuchi's LOC design in Russell's package.

Response to Arguments

3. Applicant's arguments filed on 07-29-02 have been fully considered but they are not persuasive.

A. Applicant contends that Russell discloses much more than four stable leads and does not suggest using at most four such leads.

However, as explained above, Tsubosaki et al teach using a variety of configurations of a LOC device having support/stable/bus bar leads where the LOC device is supported by two support/stable leads (3C in Fig. 15 and 17; Col. 9, line 60-Col. 10, line 25). Therefore, Tsubosaki et al's lead structure is applied to Russell's LOC device.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

10-16-02

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800